



SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Applicant : Michael Smith, et al.
 App. No : 10/712,212
 Filed : November 13, 2003
 For : STRUCTURE AND METHOD OF
 FABRICATING A TRANSISTOR
 HAVING A TRENCH GATE
 Examiner : Allan R. Wilson
 Art Unit : 2815

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

4/29/05

(Date)

John R. King

John R. King, Reg. No. 34,362

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Supplemental Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing 1 reference to be considered by the Examiner. Also enclosed is 1 foreign patent references and/or non-patent literature as listed on the Supplemental Information Disclosure Statement.

This Supplemental Information Disclosure Statement is being filed before the mailing date of a final action and before the mailing of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 C.F.R. § 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

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Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 4/29/05

By: John R. King
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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | Application No. | 10/712,212 |
| | | Filing Date | November 13, 2003 |
| | | First Named Inventor | Michael Smith |
| | | Art Unit | 2815 |
| (Multiple sheets used when necessary) | | Examiner | Allan R. Wilson |
| SHEET 1 OF 1 | | Attorney Docket No. | MICRON.271A |

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PATENT & TRADEMARK OFFICE*

| U.S. PATENT DOCUMENTS | | | | |
|-----------------------|----------|---|--------------------------------|-------------------------------|
| Examiner Initials | Cite No. | Document Number Number - Kind Code (if known) Example: 1,234,567 B1 | Publication Date MM-DD-YYYY | Name of Patentee or Applicant |
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| FOREIGN PATENT DOCUMENTS | | | | | | |
|--------------------------|----------|--|-----------------------------------|----------------------------------|--|----------------|
| Examiner Initials | Cite No. | Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1 | Publication Date MM-DD-YYYY | Name of Patentee or Applicant | Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear | T ¹ |
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| NON PATENT LITERATURE DOCUMENTS | | | | | | |
|---------------------------------|----------|---|--|--|--|----------------|
| Examiner Initials | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | | T ¹ |
| | | Sakao, et al. A STRAIGHT-LINE TRENCH ISOLATION AND TRENCH-GATE TRANSISTOR (SLIT) CELL FOR GIGA-BIT DRAMS; ULSI Device Development Laboratories, NEC Corporation; 1120, Shimokuzawa, Sagamihara, Kanagawa 229, Japan; "1993 Symposium on VLSI Technology, Digest of Technical Papers," Pages 19 and 20 | | | | |

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|--|-----------------|
| Examiner Signature | Date Considered |
| *Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | |

¹ - Place a check mark in this area when an English language Translation is attached.